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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/599,264	09/25/2006	Martin J. Edwards	GB 040069	6370

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EXAMINER	
NGUYEN, KHAI M	
ART UNIT	PAPER NUMBER
2819	

NOTIFICATION DATE	DELIVERY MODE
04/21/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No.	Applicant(s)	
	10/599,264	EDWARDS, MARTIN J.	
	Examiner	Art Unit	
	KHAI M. NGUYEN	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 7-12, 15-16, 20-21, 24-25, and 30-33* is/are rejected.

7)☒ Claim(s) *2-6, 13-14, 17-19, 22-23, and 26-29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *6/15/2008* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. Figures 1-2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The application has not been checked to the extent necessary to determine the presence of all possible typographical and grammatical errors. However, Applicant's cooperation is requested in correcting any errors of which he/she may become aware in the application.

4. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Claim Objections

5. Claim 7 is objected to because of the recitation "wherein the plurality of the capacitor circuits comprises all but one of the capacitor circuits" is unclear to the examiner. Clarification is required.

6. Claim 8 is objected to because of the recitation "wherein said one input circuit is controlled by..." is unclear to the examiner – it is not clear what "one input circuit' is being referred to. Clarification is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 7-12, 15-16, 20-21, 24-25, and 30-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Edwards (US 6,169,508).

Regarding claim 1, Edwards discloses a digital to analogue converter (8-bit DAC 10 of Fig. 1 – see, title, abstract, and col. 3, lines 7-9) comprising:

a plurality of digital inputs (D0-D5 = 6-LSB bits of the 8-bit DAC 10 → col. 3, lines 7-9) corresponding in number to the number of bits of a digital input word (serial data at terminal 16 of Fig. 1), the inputs (6-LSB bits) being used to select one of first and second binary voltage levels (Vl and Vh provided by 34 of Fig. 1 → col. 3, lines 22-25) (VH,VL) as binary inputs to the converter;

a respective capacitor circuit (C, 2C, ..., 32C of weighted capacitor bank or network 20 of Fig. 1) associated with each input (col. 3, lines 23-41);

first and second clock inputs (CKI, CK2 – control line 44 of Fig. 1 → col. 3, lines 42-48, and col. 4, lines 10-13);

an output load (Cc of Fig. 1 – col. 3, lines 38-41); and

a plurality of switches (charging switches 36 and output switches 42 of Fig. 1) controlled by the clock inputs (on the control line 44) for controlling the coupling of the

capacitor circuits either to one of the binary inputs or to the output load (col. 3, lines 42-48, and col. 4, lines 10-13),

wherein a plurality of the capacitor circuits (including the weighted capacitor network 20 and switches 32, 36, and 42 of Fig. 1) are controllable to output an effective voltage to the load comprising the first binary voltage level, the second binary voltage level or an average of the first and second binary voltage levels in dependence on the bits of the digital input word (col. 3, lines 14-67; col. 1, lines 4-18).

Regarding claim 7, Edwards discloses a converter as claimed in claim 1, wherein the plurality of the capacitor circuits comprises all but one of the capacitor circuits (including circuits 32/34 of Fig. 1).

Regarding claim 8, Edwards discloses a converter as claimed in claim 1, wherein said one input circuit (32) is controlled by the most significant bit (D5 of the 6-LSB bit of claim 1) of the digital input word.

Regarding claim 9, Edwards discloses a converter as claimed in claim 1, wherein said one capacitor circuit (e.g., 32C) is controllable (by signal on line 44 of Fig. 1) to output an effective voltage comprising only the first binary voltage level (VH) or the second binary voltage level (VL) (col. 4, lines 4-18).

Regarding claim 10, Edwards discloses a converter as claimed in claim 1, wherein the capacitor circuits (as seen the weighted capacitor network 20 of Fig. 1) are connected in parallel between the plurality of inputs (32) and the capacitive output load (50 of Fig. 1).

Regarding claim 11, Edwards discloses a converter as claimed in claim 1, wherein each of the capacitor circuits comprises an input switch (a charging switch 36) and an output switch (an output switch 42) in series (see Fig. 1) between one of the binary inputs (from 32) and the output load (50), and further comprising a capacitor (C, 2C…) connected between the junction between the input switch and output switch and a common terminal.

Regarding claim 12, Edwards discloses a converter as claimed in claim 11, wherein each input switch (36) is controlled by the first clock input and each output switch (42) is controlled by the second clock input (col. 3, lines 42-47; col. 4, lines 4-18).

Regarding claim 15, Edwards discloses a converter as claimed in claim 1, wherein each of the capacitor circuits comprises an input switch and an output switch (including switches 33a/33b and/or 36/42) in series between a first power line (20 = Vh of Fig. 1) and a second power line (22 = Vl of Fig. 1), wherein the first power line is selectively connected to the first binary voltage level (Vh) and the second power line is selectively connected to the second binary voltage level (Vl), and further comprising a

capacitor (one of the weighted capacitors in the capacitor network 20 of Fig. 1) connected between the junction between the input switch and output switch (including switches 33a/33b and/or 36/42) and a common terminal (50 of Fig. 1).

Regarding claim 16, Edwards discloses a converter as claimed in claim 1, wherein the input switches (switches 33a of 32 of Fig. 1) are each controlled by a respective digital input (DO - D5 – i.e., the 6-LSB bits from latch 6 of fig. 1) and the output switches (switches 33b of Fig. 1) are each controlled by the complement (/DO - /D5 - i.e., each of the 6-LSB bits from latch 6 is inverted/complemented before being provided to switches 33b → as seen, each of switches 33b has an inverter) of the respective digital input (6-LSB bits).

Regarding claim 20, Edwards discloses a converter as claimed in claim 1, wherein each capacitor circuit (each including a weighted capacitor of the capacitor network 20 and pair of switches 36/42 of Fig. 1) has an effective resistance determined by the capacitance (and that is driven by frequency of a clock line 44 of Fig. 1).

Regarding claim 21, Edwards discloses a converter as claimed in claim 20, wherein the capacitor circuits (20 of Fig. 1) have effective resistances (R, 2R, ..., 32R) such that they form a binary weighted circuit configuration (C, 2C, 4C…32C).

Regarding claim 24, Edwards discloses a converter as claimed in claim 1, wherein the capacitor circuits (capacitor network 20 of Fig. 1) are connected in parallel between the plurality of inputs (inputs of 40 of Fig. 1) and junctions of a resistor chain (R – output side of 40), a first end of the resistor chain being connected to the output load (50).

Regarding claim 25, Edwards discloses a converter as claimed in claim 24, wherein the capacitor circuits (20 of Fig. 1) have the same effective resistances (2R – resistance of 20 is determined by capacitance of the weighted capacitors and frequency on line 44).

Regarding claim 30, Edwards discloses a method of performing digital to analogue conversion (see, DAC of Fig. 1), comprising:

using the bits of a digital input word (8-bit input – col. 3, lines 5-10) to generate a plurality of control voltages (col. 3, lines 14-22) corresponding in number to the number of bits (two MSB bits), one control voltage comprising a first binary voltage level or a second binary voltage level, and each other control voltage comprising a first binary voltage level, a second binary voltage level or an average of the first and second binary voltage levels (col. 3, lines 5-22); and

using the plurality of control voltages (V1…V5) to drive an output load (load that is connected to node 50 of Fig. 1 – col. 3, lines 35-48).

Regarding claim 31, Edwards discloses a method as claimed in claim 30, wherein generating (by circuit 34 of Fig. 1) a plurality of control voltage comprises operating a switched capacitor resistor circuit (line 15 of col. 3 to line 18 of col. 4).

Regarding claim 32, Edwards discloses a method as claimed in claim 30, wherein generating (by circuit 34 of Fig. 1) a plurality of control voltage comprises (Vl, Vh) operating a plurality of switched capacitor resistor circuits (32/36/42,20 of Fig. 1) each having two control inputs, wherein one of the first and second binary voltage levels (Vl and Vh) is applied to the first control input and one of the first and second binary voltage levels is applied to the second control input (when switch 33a is closed and switch 33b is open or vice versa).

Regarding claim 33, Edwards discloses a display device (Fig. 3 – col. 6, lines 54-67) comprising: an array (34 = 82 of Fig. 3) of display pixels (80); row driver circuitry (30 = 90 of Fig . 3) for providing signals (84) to the rows of pixels (80); and column address circuitry (32 = 98 of Fig. 3) providing pixel drive signals (86) to the columns of pixels (80), wherein the column address circuitry (32 = 98) comprises a digital to analogue converter as claimed in claim 1 (col. 7, lines 3-38) .

Allowable Subject Matter

8. Claims 2-6, 13-14, 17-19, 22-23, and 26-29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form

including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record was not seen to teach or suggest the recited limitations including, separately among other things, each of the plurality of capacitor circuits includes an input circuit, having: a first branch between a first input and the output and comprising first and second switches in series; a second branch between a second input and the output and comprising third and fourth switches in series; and a capacitor connected between the junction between the first and second switches and the junction between the third and fourth switches.

Prior Art

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclose (notes: all references cited on PTO-892 Form attached herewith).

Contact Information

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khai M. Nguyen whose telephone number is 571-272-1809. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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